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(54) Software-based temperature controller circuit in an electronic apparatus

(57) The central processing unit (CPU) (17) is allowed to utilize the temperature information signal, identifying the temperature, so as to commence an interruption processing for controlling the temperature. During implementation of the interruption processing, the CPU (17) is designed to recognize the status of a cooling device (32) in accordance with a status information signal. If a failure or defect is found in the cooling device (32), a thinned-out clock signal or a clock signal of a lower frequency is supplied to the CPU (17) so as to suppress the operation of the CPU. Heat generated at the CPU can be suppressed. Additional hardware is not required to accompany the CPU (17) so as to solely generate an interrupt request signal based on the status of the cooling device (32). The circuit structure of the temperature controller circuit can be simplified.

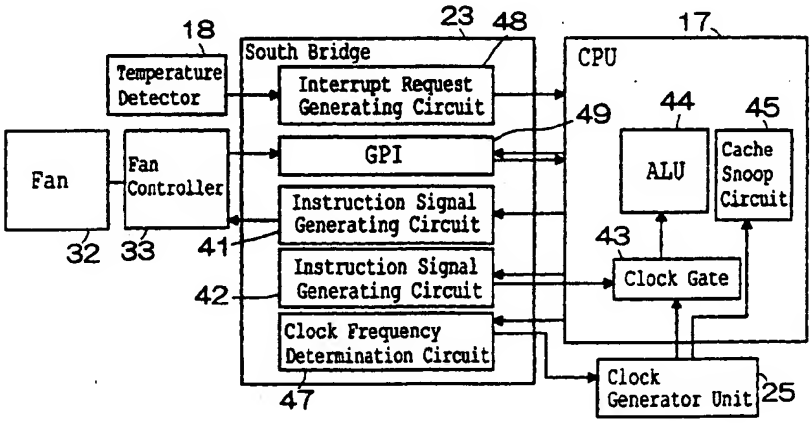

Fig.3

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Description

[0001] The present invention relates to a method of controlling temperature in an electronic apparatus such as a computer device, more particularly, to a method of changing the operation of a central processing unit (CPU) based on an information signal identifying the status of a cooling device such as a cooling fan installed within the computer device.

[0002] In general, a cooling fan is disposed within an enclosure of a computer system. The cooling fan is designed to generate air stream for taking out heat from a CPU and for blowing it out of the enclosure. The air stream serves to suppress the interior temperature of the enclosure from increasing. Employment of no cooling fan induces an excessive temperature increase within the enclosure, so that the CPU and other electronic components in the vicinity of the CPU may suffer from a defect or failure of operation.

[0003] If the cooling fan fails to properly operate, the heat generated at the CPU cannot be released out of the enclosure enough. In this case, the operation of the CPU is preferably suppressed to reduce the generated heat so that the increase can be avoided in the interior temperature. The suppression can be achieved by a reduced or thinned-out frequency of the clock signal supplied to the CPU, for example.

[0004] When the operation of the CPU is to be suppressed, the CPU is expected to receive an interrupt request IRQ for identifying defect or failure of the cooling fan. When the CPU receives the interrupt request IRQ, the CPU is designed to temporarily discontinue the current primary processing so as to realize establishment of a reduced or thinned-out frequency of the clock signal in an interruption processing. As a result of suppression of the operation in the CPU in this manner, an excessive increase can be prevented in the interior temperature of the enclosure.

[0005] The interrupt request IRQ is usually supplied from a system controller such as a chipset, for example. The system controller is thus required to include a hardware or electronic component for generating an interrupt request IRQ. The circuit structure of the system controller inevitably gets complicated. In addition, reduction in size cannot be achieved in the system controller due to the hardware for generating an interrupt request IRQ.

[0006] An embodiment of the present invention may provide a temperature controller circuit capable of managing the interior temperature of an electronic apparatus with a simpler circuit structure, and a method therefor.

[0007] According to the present invention, there is provided a temperature controller circuit for an electronic apparatus, comprising: a central processing unit (CPU); an interrupt request generating unit generating an interrupt request signal based on a temperature information signal identifying a temperature and designed to output the interrupt request signal to the central processing unit; and an input unit designed to supply to the central processing unit a status information signal identifying status of a cooling device.

[0008] Employment of the above-described temperature controller circuit may serve to implement a method of controlling temperature in an electronic apparatus according to the present invention. The method may comprise: obtaining an interrupt request signal based on a temperature information signal for identifying a temperature; obtaining a status information signal for identifying status of a cooling device in response to reception of the interrupt request signal; and changing operation of an electronic device (e.g. CPU) based on the status information signal.

[0009] With the above-described method, a central processing unit (CPU) is allowed to utilize the temperature information signal, identifying the temperature, so as to commence an interruption processing for controlling the temperature. During the interruption processing, the CPU is designed to recognize the status of the cooling device in accordance with the status information signal. Additional hardware is not required to accompany the CPU so as to solely generate an interrupt request signal based on the status of the cooling device. The circuit structure of the temperature controller circuit can be simplified.

[0010] In general, in the case where the cooling device is employed to control the temperature in the electronic apparatus, a failure or defect of the cooling device can be ignored if the temperature is properly controlled, in other words, if the temperature stays below a predetermined temperature. If an interrupt request signal is designed to be generated in response to the failure or defect of the cooling device as is conventionally known, the operation of the CPU is correspondingly interrupted irrespective of the proper temperature in the electronic apparatus. On the other hand, according to the present invention, the temperature information signal is designed to trigger the generation of the interrupt request signal, so that the CPU is reliably prevented from suffering from a frequent interruption during the operation as long as the temperature is properly controlled irrespective of a failure or defect of the cooling device.

[0011] A temperature detector or thermal sensor may be connected to the interrupt request generating unit so as to measure the actual temperature within the enclosure of the electronic apparatus. The thermal sensor serves to achieve a proper generation of the interrupt request signal in correspondence with variation in the actual temperature within the enclosure of the electronic apparatus. The control of the cooling device based on the thus generated interrupt request signal serves to avoid an excessive increase in the temperature within the enclosure of the electronic apparatus. The thermal sensor may be designed to directly measure the temperature of the CPU.

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[0012] For example, the input unit may comprise a general purpose input (GPI) circuit incorporated within a system controller (chipset) or a so-called ultra I/O (Input/Output). The system controller and the ultra I/O are in general designed to support the operation of the CPU. The system controller may comprise a north bridge connected to the CPU through a system bus, and a south bridge connected to the north bridge through a PCI bus, for example.

[0013] The cooling device may include a cooling fan designed to generate air stream for taking out heat from the CPU, for example. However, the cooling device is not limited to the cooling fan. The cooling device is only required to prevent an excessive increase in the temperature within the enclosure of the electronic apparatus by any means.

[0014] In the aforementioned method, the operation of the CPU may be suppressed in response to reception of the status information signal identifying a failure or defect of the cooling device. The suppression in the operation of the CPU serves to suppress heat generated at the CPU. Accordingly, an increase in the temperature within the enclosure can be suppressed. The suppressed operation of the CPU may also be achieved when the status information signal identifies a compulsory termination of the operation of the cooling device due to an intentional reduction in energy consumption.

[0015] In the aforementioned method, a thinned-out clock signal may be supplied to the central processing unit so as to suppress the operation of the central processing unit. Likewise, a clock signal of a lower clock frequency may be supplied to the central processing unit so as to suppress the operation of the central processing unit. Otherwise, a software managing the overall system such as an operating system (OS) may be suspended or shut down in suppressing the operation of the CPU.

[0016] Furthermore, the aforementioned method may be realized by a computer software such as a BIOS (Basic Input/Output System). The computer software may be installed to the computer system from a portable storage medium such as a magnetic disk, including an FD (floppy disk), an optical disk, including a CD (compact disk), or the like. Alternatively, the computer software may be installed to the computer system through a network such as the Internet.

[0017] A preferred embodiment of the invention will now be described in conjunction with the accompanying drawings, wherein:

Fig. 1 illustrates the overall appearance of a notebook type personal computer;

Fig. 2 is a block diagram schematically illustrating the circuit structure of a motherboard;

Fig. 3 is a block diagram schematically illustrating the structure of a south bridge;

Fig. 4 is a flowchart illustrating an example of an interruption processing;

Fig. 5 is a time chart illustrating the concept of a thinned-out clock signal;

Fig. 6 is a flowchart illustrating another example of the interruption processing;

Fig. 7 is a flowchart illustrating a further example of the interruption processing;

Fig. 8 is a flowchart illustrating a still further example of the interruption processing; and

Fig. 9 is a time chart schematically illustrating the advantage of a threshold temperature for a temperature rise which is higher than a threshold temperature for a temperature drop.

[0018] Fig. 1 schematically illustrates a notebook type personal computer 10 as an electronic apparatus; The personal computer 10 comprises a main enclosure 11 in which a central processing unit (CPU) and other electronic components are incorporated, and a lid 12 connected to the main enclosure 11. A liquid crystal display (LCD) and the like is incorporated in the lid 12. The lid 12 is allowed to swing, relative to the main enclosure 11, about the support axis. The swinging movement of the lid 12 is designed to cause the lid 12 to be superposed on the main enclosure 11.

[0019] Input devices such as a keyboard 13 and a pointing device 14 are mounted over the upper surface of the main enclosure 11. When application software is executed in the personal computer 10, an operator is expected to manipulate the keyboard 13 and/or the pointing device 14 so as to input required information and/or instructions. Processing and/or results of execution of the application software may be displayed on the screen of the LCD incorporated in the lid 12.

[0020] Fig. 2 schematically illustrates the circuit structure of a printed circuit board unit such as a motherboard 16 incorporated within the main enclosure 11. A CPU 17 is mounted on the motherboard 16 for executing application software on an operating system (OS), for example. A surface mount technique may be employed to mount the CPU 17 on the motherboard 16. Alternatively, the CPU 17 may be received within a CPU slot fixedly mounted on the motherboard 16.

[0021] A temperature detector or thermal sensor 18 is embedded within a silicon body of the CPU 17 for detecting a temperature of the CPU 17. The temperature detector 18 is designed to generate a temperature information signal identifying the temperature of the CPU 17. In generation of the temperature information signal, the temperature detector 18 compares a measured actual temperature with a predetermined threshold temperature. When the measured actual temperature exceeds the predetermined threshold temperature, the temperature detector 18 is allowed to keep outputting a notification signal of a high level. When the measured actual temperature stays below the predetermined threshold temperature, however, the temperature detector 18 is allowed to keep outputting the notification signal of a low level. The predetermined threshold

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temperature may be determined based on a highest permissible temperature for guaranteeing a reliable operation of the CPU 17 and other electronic components in the vicinity of the CPU 17.

[0022] A system controller such as a chipset 19 is connected to the CPU 17. The chipset 19 is designed to manage the overall system of the personal computer 10. The chipset 19 comprises, for example, a north bridge 21 connected to the CPU through a system bus 20, and a south bridge 23 connected to the north bridge 21 through a so-called PCI (Peripheral Component Interconnect) bus 22.

[0023] A system memory unit 24 is connected to the north bridge 21. The north bridge 21 serves to allow the CPU 17 to fetch programs of the OS and/or application software temporarily stored in the system memory unit 24. Memory modules such as a synchronous dynamic random access memory (SDRAM) can be employed as the system memory unit 24. The memory modules may be received within corresponding DIMM (dual in-line memory module) connectors fixedly mounted on the motherboard 16, for example.

[0024] A clock signal is supplied to the CPU 17 and the system memory unit 24, respectively. The clock signal is generated at a clock generator unit or circuit 25. The operational speed of the CPU 17 can be determined by the frequency of the clock signal. The clock signal may be supplied to the north and south bridges 21, 23 and other electronic components or elements, in addition to the CPU 17 and the system memory unit 24. As a result, the north and south bridges 21, 23 and the other electronic components are designed to operate in synchronization with the operation of the CPU 17.

[0025] A so-called IDE (Integrated Device Electronics) connector 26 is connected to the south bridge 23 so as to establish an IDE interface. For example, the IDE connector 26 allows for connection of a large-capacity storage device such as a hard disk drive (HDD) 27 assembled within the main enclosure 11. When the CPU 17 executes an application software, for example, the south bridge 23 serves to transfer programs and/or data, read out of the HDD 21, to the system memory unit 24.

[0026] A PCMCIA (Personal Computer Memory Card International Association) controller unit 28 and a modem 29 are respectively connected to the PCI bus 22. A PC card slot is electrically connected to the PCMCIA controller unit 28. When a PC card is received in the PC card slot, as is conventionally known, a specific interface such as an IDE or SCSI interface can be established between the north bridge 21 and an exterior peripheral device such as a compact disk (CD) drive 31, including a CD-ROM or CD-R or CD-RW drive. In addition, a phone or communication line can be connected to the modem 29. The line may be wired or wireless. The modem 29 serves to connect the CPU 17 to a network such as the Internet, an extranet, or the like.

[0027] A cooling device such as a cooling fan 32 is incorporated within the main enclosure 11 for generating air stream. The generated air stream is expected to escape out of the main enclosure 11 after absorbing heat within the main enclosure 11. The cooling fan 32 is expected to suppress an increase in the interior temperature of the main enclosure 11. A fan controller unit or circuit 33 serves to control the operation or rotation of the cooling fan 32. The fan controller unit 33 is designed to output an alarm signal when it detects any defect or failure in the operation or rotation of the cooling fan 32.

[0028] A so-called ultra I/O (input/output circuit or unit) 35 is connected to the south bridge 23 through a so-called ISA (Industry Standard Architecture) bus 34. A pin terminal for the keyboard 13, a so-called PS/2 (Personal System/2) connector 36 for receiving a connector terminal of the pointing device 14, and a so-called FDD (Floppy Disk Drive) connector 38 for receiving a connector terminal of an FDD 37, are respectively connected to the ultra I/O 35. Moreover, a PS/2 connector for receiving a connector terminal of an additional external keyboard, or a PS/2 connector for receiving a connector terminal of an external mouse device, both not shown, may likewise be connected to the ultra I/O 35.

[0029] A so-called flash memory (EEPROM: electrically erasable and programmable ROM, for example) 39 is connected to the ultra I/O 35 for storing a BIOS (Basic Input/Output System). The CPU 17 is designed to manage the input/output operation between the OS and the fundamental peripheral devices such as the LCD, the keyboard 13, the pointing device 14, the HDD 27, and the like, in accordance with the BIOS read out from the flash memory 39.

[0030] As shown in Fig. 3, the south bridge 23 comprises an instruction signal generating circuit 41 designed to generate a fan instruction signal in accordance with instructions issued from the CPU 17. The fan instruction signal may include a trigger information signal for identifying an instruction to start or terminate a rotation of the cooling fan 32, a numerical information signal for identifying the rotation speed to be set at the cooling fan 32, and the like. The fan controller unit 33 is designed to control the operation or rotation of the cooling fan 32 in accordance with the instruction and the number identified in the fan instruction signal.

[0031] An instruction signal generating circuit 42 is likewise designed to generate a clock-gate instruction signal STPCLK# in accordance with instructions issued from the CPU 17. The clock-gate instruction signal STPCLK# may include information for identifying whether or not the clock signal is thinned out, how many clocks are made inoperative when the clock signal is thinned out, and the like. A clock gate 43 of the CPU 17 is designed to realize a thinned-out or a throttled clock signal in accordance with the information included in the received clock-gate instruction signal STPCLK#.

[0032] If a normal clock signal, without being thinned out or throttled, is supplied to the CPU 17, the

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CPU 17 is allowed to operate at the maximum operational speed which is inherent to the clock frequency of the clock signal. For example, when the clock gate 43 receives the clock-gate instruction signal STPCLK# identifying the "10% thinned-out," the clock gate 43 is adapted to alternately realize supply of the clock signal for 90ns and interruption of the supply for 10ns. Accordingly, an ALU (arithmetical and logical unit) 44 is caused to alternately repeat the continuation and the discontinuation of the operation by the ratio of 9 to 1. The load to the ALU 44 can be suppressed to 90% of the maximum load permissible to the ALU 44. Such suppression in the load of the ALU 44 is expected to contribute to suppression of heat generated at the CPU 17. It should be noted that the thinned-out or throttled clock signal can be supplied to electronic components, including the ALU 44, which are designed to accept an intermittent operation, while the thinned-out clock signal cannot be supplied to electronic components, such as a cache snoop circuit 45, which are required to keep operating.

[0033] A clock frequency determination circuit 47 is designed to generate a clock frequency determination signal in accordance with instructions issued from the CPU 17. The clock frequency determination signal may include information for identifying the clock frequency of the clock signal. The clock generator unit 25 is designed to output the clock signal at the clock frequency identified in the received clock frequency determination signal. The clock frequency can be switched over between the maximum or highest frequency allowing the CPU 17 to operate at the maximum operational speed and a low frequency set lower than the maximum frequency. When the CPU 17 operates in response to the clock signal of the low frequency, it is expected that heat generated at the CPU 17 can be suppressed as compared with the case where the CPU 17 operates at the maximum operational speed.

[0034] An interrupt request generating circuit 48 is designed to generate an interrupt request signal INTR when it detects a rise to the high level or a drop to the low level in the notification signal issued from the temperature detector 18. The interrupt request signal INTR is supplied to the CPU 17. When the CPU 17 receives the interrupt request signal INTR, the CPU 17 is forced to interrupt the current processing so as to thereafter execute an interruption processing assigned to the interrupt request signal INTR. In place of the interrupt request signal INTR, a SMI# signal (System Management Interrupt signal) of a higher priority can be employed to trigger the execution of the interruption processing in the CPU 17.

[0035] A GPI (General Purpose Input) circuit 49 comprises a register, not shown, designed to hold a binary data, namely, a value "0" or a value "1" in accordance with the presence of the alarm signal supplied from the fan controller unit 33. The CPU 17 is allowed to fetch the binary data out of the register. The fetched binary data may comprise a status information signal identifying the status of the cooling fan 32.

[0036] Now, when the personal computer 10 is booted up, the CPU 17 starts to operate based on the OS read out of the HDD 27 and the BIOS read out of the flash memory 39. The CPU 17 is designed to cause the instruction signal generating circuit 41 of the south bridge 23 to output the fan instruction signal. If the CPU 17 executes an application software under a heavy load, a greater amount of heat may be generated by the operating CPU 17. The heat may be transferred to air surrounding the CPU 17. A temperature rise results in the confined space of the main enclosure 11. Rotation of the cooling fan 32 serves to generate air circulation between the interior and exterior of the main enclosure 11. The interior temperature of the main enclosure 11 is thus avoided from increasing too far.

[0037] During the operation of the CPU 17, the temperature detector 18 keeps monitoring the actual temperature of the CPU 17. Assume that the measured actual temperature of the CPU 17 exceeds the predetermined threshold temperature in response to the increased heat at the CPU 17. When the measured actual temperature has exceeded the level of the predetermined threshold temperature, the notification signal generated at the temperature detector 18 is changed over from the low level to the high level. The interrupt request generating circuit 48 of the south bridge 23 outputs the interrupt request signal INTR to the CPU 17 in response to the rise from the low level to the high level in the notification signal.

[0038] The CPU 17 is then caused to interrupt the current primary processing in response to the received interrupt request signal INTR. Thereafter, the CPU 17 starts to execute the interruption processing in accordance with the BIOS read out of the flash memory 39. When the CPU 17 executes the interruption processing, as shown in Fig. 4, the CPU 17 is designed to first determine whether the interrupt request signal INTR is output in response to the temperature, rise exceeding the threshold temperature or the temperature drop falling below the threshold temperature, at step *S1*, for example. The determination of the CPU 17 can be achieved by counting reception of the interrupt request signals INTR, for example, since the CPU 17 is only allowed to alternately receive the interrupt request signals INTR for temperature rises and drops. Otherwise, the determination of the CPU 17 may be achieved by referring to the measured temperature at the temperature detector 18 in response to reception of the interrupt request signal INTR.

[0039] When the temperature rise has been recognized, the CPU 17 refers to the binary data of the register in the GPI circuit 49 at step *S2*. If the cooling fan 32 normally operates, the value "0" has been established in the register of the GPI circuit 49. The CPU 17 is thus designed to instruct generation of a clock signal, thinned out at a low rate, for achieving the moderate suppression of load at the CPU 17, at step *S3*. The

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instruction signal generating circuit 42 of the south bridge 23 generates the clock-gate instruction signal STPCLK# identifying the "10% thinned-out" in accordance with the instruction issued from the CPU 17, for example. The generated clock-gate instruction signal STPCLK# is supplied to the clock gate 43.

[0040] The clock gate 43 outputs the thinned out or throttled clock signal, as shown in Fig. 5, for example, in response to reception of the clock-gate instruction signal STPCLK#. The clock for 10% of a cyclic period is made ineffective in the thinned-out clock signal. Accordingly, the ALU 44 is allowed to alternately achieve the continuation and discontinuation of the operation in response to the supply of the effective and ineffective clock included in the thinned-out clock signal. The load to the ALU 44 can be suppressed to 90% of the maximum load permissible to the ALU 44. Although the CPU 17 operates at a low operational speed, heat generated at the CPU 17 can be suppressed. The thinned-out clock signal serves, in combination with a cooling performance achieved by the cooling fan 32, to prevent the interior temperature of the main enclosure 11 from increasing. The CPU 17 then completes the interruption processing. The CPU 17 is thereafter allowed to start a continuation of the interrupted primary processing.

[0041] Referring again to Fig. 4, the CPU 17 is designed to fetch the value "1" from the register of the GPI circuit 49, at step *S2*, if the alarm signal is output from the fan controller unit 33. As a result, the CPU 17 detects a failure in the operation of the cooling fan 32. Otherwise, if the cooling fan 32 is intended to stop rotating so as to achieve suppression in energy consumption, the value "1" can be established in the register of the GPI circuit 49.

[0042] When a failure has been found in the operation of the cooling fan 32 in the aforementioned manner, the CPU 17 is designed to instruct generation of a clock signal, thinned out at a high rate, for achieving the tight or strong suppression of load at the CPU 17, at step *S4*. The instruction signal generating circuit 42 of the south bridge 23 generates the clock-gate instruction signal STPCLK# identifying the "30% thinned-out" in accordance with the instruction issued from the CPU 17, for example. The generated clock-gate instruction signal STPCLK# is supplied to the clock gate 43.

[0043] The clock gate 43 outputs the thinned out or throttled clock signal, as shown in Fig. 5, for example, in response to reception of the clock-gate instruction signal STPCLK#. The clock for 30% of a cyclic period is made ineffective in the thinned-out clock signal. Accordingly, the ALU 44 is allowed to alternately achieve the continuation and discontinuation of the operation in response to the supply of the effective and ineffective clock included in the thinned-out clock signal. The load on the ALU 44 can remarkably be suppressed to 70% of the maximum load permissible on the ALU 44. Heat generated at the CPU 17 can be greatly suppressed as compared with the case achieved by the aforementioned 10% thinned-out clock signal. Without a cooling performance achieved by the cooling fan 32, the thinned-out clock signal solely serves to prevent the interior temperature of the main enclosure 11 from increasing. The CPU 17 then completes the interruption processing. The CPU 17 is thereafter allowed to start a continuation of the interrupted primary processing.

[0044] Next, assume that a cooling performance achieved by the cooling fan 32 and/or the thinned-out clock signal sufficiently reduces the interior temperature of the main enclosure 11 during the continuation of the interrupted primary processing. When the measured actual temperature has dropped below the predetermined threshold temperature, the notification signal generated at the temperature detector 18 is changed over from the high level to the low level. The interrupt request generating circuit 48 of the south bridge 23 outputs the interrupt request signal INTR to the CPU 17 in response to the drop from the high level to the low level in the notification signal.

[0045] The CPU 17 is then caused to interrupt the current primary processing in response to the received interrupt request signal INTR. Thereafter, the CPU 17 starts to execute the interruption processing in accordance with the BIOS read out of the flash memory 39. Here, when the temperature drop is recognized at step *S1*, the CPU is designed to instruct cancellation of the thinned-out clock signal without referring to the binary data of the register in the GPI circuit 49 at step *S5*. The instruction signal generating circuit 42 of the south bridge 23 generates the clock-gate instruction signal STPCLK# identifying the "0% thinned out," namely, the clock without being thinned out, in accordance with the instruction issued from the CPU 17. The generated clock-gate instruction signal STPCLK# is supplied to the clock gate 43. The clock gate 43 accordingly terminates the output of the thinned-out clock signal and starts outputting the normal continuous clock signal. The CPU 17 then completes the interruption processing. The CPU 17 is thereafter allowed to start a continuation of the interrupted primary processing. The ALU 44 is expected to bear the maximum load during operation.

[0046] In place of the aforementioned thinned-out clock signal, the interruption processing may employ the change in the clock frequency of the clock signal supplied to the CPU 17. As shown in Fig. 6, when the temperature rise has been recognized in the aforementioned manner at step *T1*, in the same manner as described above, the CPU 17 is designed to refer to the binary data of the register in the GPI circuit 49 at step *T2*, for example. If the value "0" has been established in the register, at step *T3*, the CPU 17 instructs generation of the clock signal having a moderate frequency, such as 400MHz, which is relatively lower than the maximum frequency, 500MHz, for example. The clock frequency determination circuit 47 of the south bridge 23 generates the clock frequency determination signal identifying the clock frequency of 400MHz in

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accordance with the instruction issued from the CPU 17. The generated clock frequency determination signal is supplied to the clock generator unit 25. The clock generator unit 25 supplies the clock signal having the clock frequency of 400MHz to the CPU 17 in accordance with the received clock frequency determination signal. Although the CPU 17 operates at a relatively low or moderate operational speed, heat generated at the CPU 17 is expected to be suppressed. The moderate clock frequency serves, in combination with a cooling performance achieved by the cooling fan 32, to prevent the interior temperature of the main enclosure 11 from increasing. The CPU 17 is allowed to complete the interruption processing in this manner.

[0047] On the other hand, when the value "1" has been confirmed in the register of the GPI circuit 49 at step *T2*, in the same manner as described above, the CPU 17 instructs generation of the clock signal having a lower frequency, such as 250MHZ, which is still lower than the aforementioned moderate frequency, for example. The clock frequency determination circuit 47 of the south bridge 23 generates the clock frequency determination signal identifying the clock frequency of 250MHz in accordance with the instruction issued from the CPU 17. The generated clock frequency determination signal is supplied to the clock generator unit 25. The clock generator unit 25 supplies the clock signal having the clock frequency of 250MHz to the CPU 17 in accordance with the received clock frequency determination signal. Although the CPU 17 operates at a remarkably lower operational speed, heat generated at the CPU 17 is expected to largely be suppressed. Without assistance of a cooling performance achieved by the cooling fan 32, the lower clock frequency solely serves to prevent the interior temperature of the main enclosure 11 from increasing. The CPU 17 is allowed to complete the interruption processing in this manner.

[0048] Thereafter, when the temperature drop has been recognized at step *T1*, in the same manner as described above, the CPU 17 instructs generation of the clock signal having the maximum frequency, 500MHz, at step *T5*. The clock frequency determination circuit 47 of the south bridge 23 generates the clock frequency determination signal identifying the clock frequency of 500MHz in accordance with the instruction issued from the CPU 17. The generated clock frequency determination signal is supplied to the clock generator unit 25. Accordingly, after completion of the interruption processing in this manner, the CPU 17 is allowed to operate at the maximum operational speed possibly achieved by the set maximum clock frequency.

[0049] The above-described interruption processing may force the personal computer 10 to be suspended or shut down, at steps *S4* and *T4*, when a failure has been found in the operation of the cooling fan 32 at steps *S2* and *T2*, as shown in Figs. 7 and 8. As is conventionally known, the operation of a so-called ATX power supply Interface, incorporated in the south bridge 23, can be utilized to suspend or shut down the personal computer 10 in the above manner, for example. If the personal computer 10 is suspended or shut down, the operation of the CPU 17 can be terminated so that heat generated at the CPU 17 can reliably be suppressed. In addition, two kinds of the thinned-out clock signal are not required in the interruption processing, as is apparent from Fig. 7, while two kinds of clock frequency for the clock signal may replace three kinds of clock frequency in the aforementioned interruption processing, as is apparent from Fig. 8.

[0050] The above-described interruption processing may be designed to set a pair of different predetermined threshold temperatures, for example, one for the temperature rise and the other for the temperature drop. Now, assume that the predetermined threshold temperature *TH* for the temperature rise is set higher than the predetermined threshold temperature *TL*. In this case, once the actual temperature rises above the threshold temperature *TH*, an insufficient up and down of the actual temperature in the range of the threshold temperature *TH* fails to cause frequent generation of the interrupt request signal INTR unless the actual temperature reaches below the threshold temperature *TL*. As compared with the case where the same value is set for the respective threshold temperatures for temperature rise and drop, generation of the interrupt request signal to be supplied to the CPU 17 can be suppressed or decreased. Accordingly, the CPU 17 is prevented from frequent interruption during the normal primary processing for executing an application software.

[0051] The BIOS for realizing the aforementioned interruption processing can be installed in the flash memory 39 from portable storage media such as an FD (floppy disk) 51 readable by the FDD 37, a CD-ROM 52 readable by the CD drive 31, or the like, as shown in Fig. 2. Alternatively, the BIOS may be installed in the flash memory 39 through a network connected to the modem 29. When the BIOS is to be installed, the CPU 17 may execute a specific software program realizing a tool for installation, for example. Such a specific software program may be fetched into the system memory unit 24 along with the BIOS prior to installation.

[0052] It should be noted that the aforementioned BIOS can be applied not only to the motherboard 16 employed in the notebook type personal computer 10 but also to a motherboard employed in a desktop personal computer in the same manner.

[0053] Furthermore, although the above-described embodiment relates to cooling of a central processing unit (CPU), the invention may be applied to cooling of any kind of heat-generating electronic device in an electronic apparatus, e.g. a graphics chip or digital signal processor (DSP). Accordingly, the expression "interrupt request signal" is not restricted to a CPU interrupt.

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Claims

1. A temperature controller circuit for an electronic apparatus, comprising:

   a central processing unit;
   an interrupt request generating unit generating an interrupt request signal based on a temperature information signal identifying a temperature and designed to output the interrupt request signal to the central processing unit; and
   an input unit designed to supply to the central processing unit a status information signal identifying status of a cooling device.

2. The temperature controller circuit according to claim 1, wherein the input unit is a general purpose input circuit.

3. The temperature controller circuit according to claim 1 or 2, wherein the temperature information signal is supplied from a temperature detector embedded in a body of the central processing unit.

4. The temperature controller circuit according to claim 3, wherein the temperature detector is designed to generate the temperature information signal based on comparison between a measured actual temperature and a predetermined threshold temperature.

5. An electronic apparatus with a cooling device, comprising:

   an enclosure;
   a central processing unit disposed within the enclosure:
   a cooling device incorporated in the enclosure;
   a temperature detector generating a temperature information signal identifying a temperature within the enclosure;
   an interrupt request generating unit generating an interrupt request signal based on the temperature information signal and designed to output the interrupt request signal to the central processing unit; and
   an input unit designed to supply to the central processing unit a status information signal identifying status of the cooling device.

6. The electronic apparatus according to claim 5, wherein the input unit is a general purpose input circuit.

7. The electronic apparatus according to claim 5 or 6, wher in the temperature detector is embedded in a body of the central processing unit.

8. The electronic apparatus according to claim 5, wherein the temperature detector is designed to generate the temperature information signal based on comparison between a measured actual temperature and a predetermined threshold temperature.

9. A method of controlling temperature in an electronic apparatus, comprising:

   obtaining an interrupt request signal based on a temperature information signal for identifying a temperature;
   obtaining a status information signal for identifying status of a cooling device in response to reception of the interrupt request signal; and
   changing operation of the electronic apparatus based on the status information signal.

10. The method of controlling temperature according to claim 9, wherein the operation of the electronic apparatus is suppressed when a failure in operation of the cooling device is identified in the status information signal.

11. The method of controlling temperature according to claim 10, wherein the electronic apparatus comprises a heat-generating electronic device, and wherein a thinned-out clock signal is supplied to the electronic device to suppress the operation thereof.

12. The method of controlling temperature according to claim 10, wherein the electronic apparatus comprises a heat-generating electronic device, and wherein a clock signal of a lower clock frequency is supplied to the electronic device to suppress the operation thereof.

13. A program for causing a computer to execute steps of:

   obtaining an interrupt request signal based on a temperature information signal for identifying a temperature; obtaining a status information signal for identifying status of a cooling device in response to reception of the interrupt request signal; and changing operation of a central processing unit based on the status information signal.

14. A computer-readable storage medium storing the program of claim 13.

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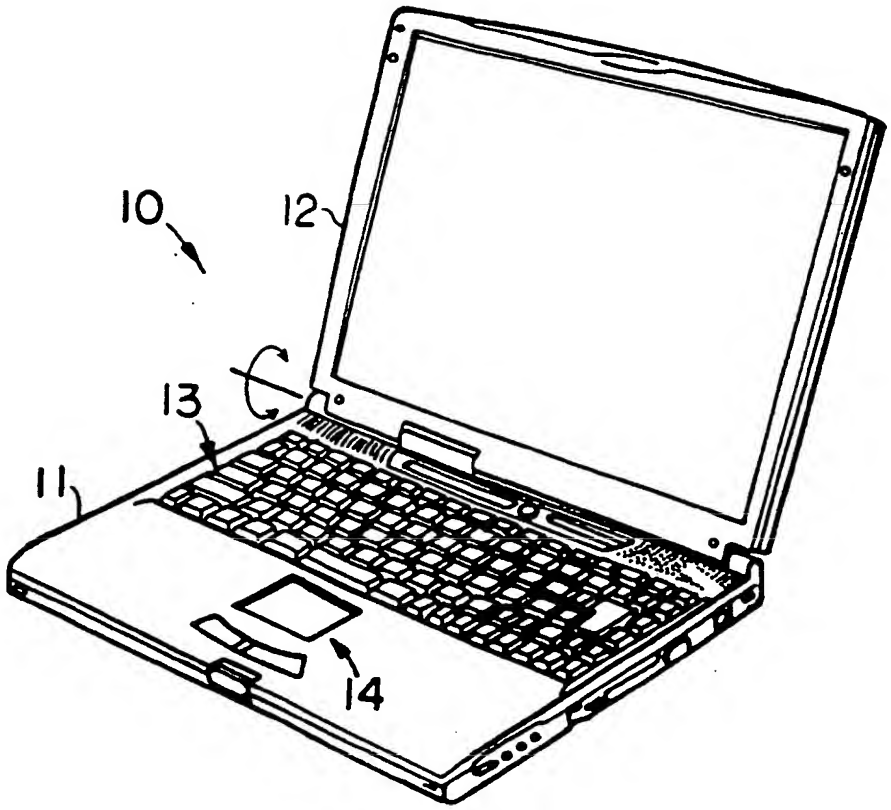

Fig.1

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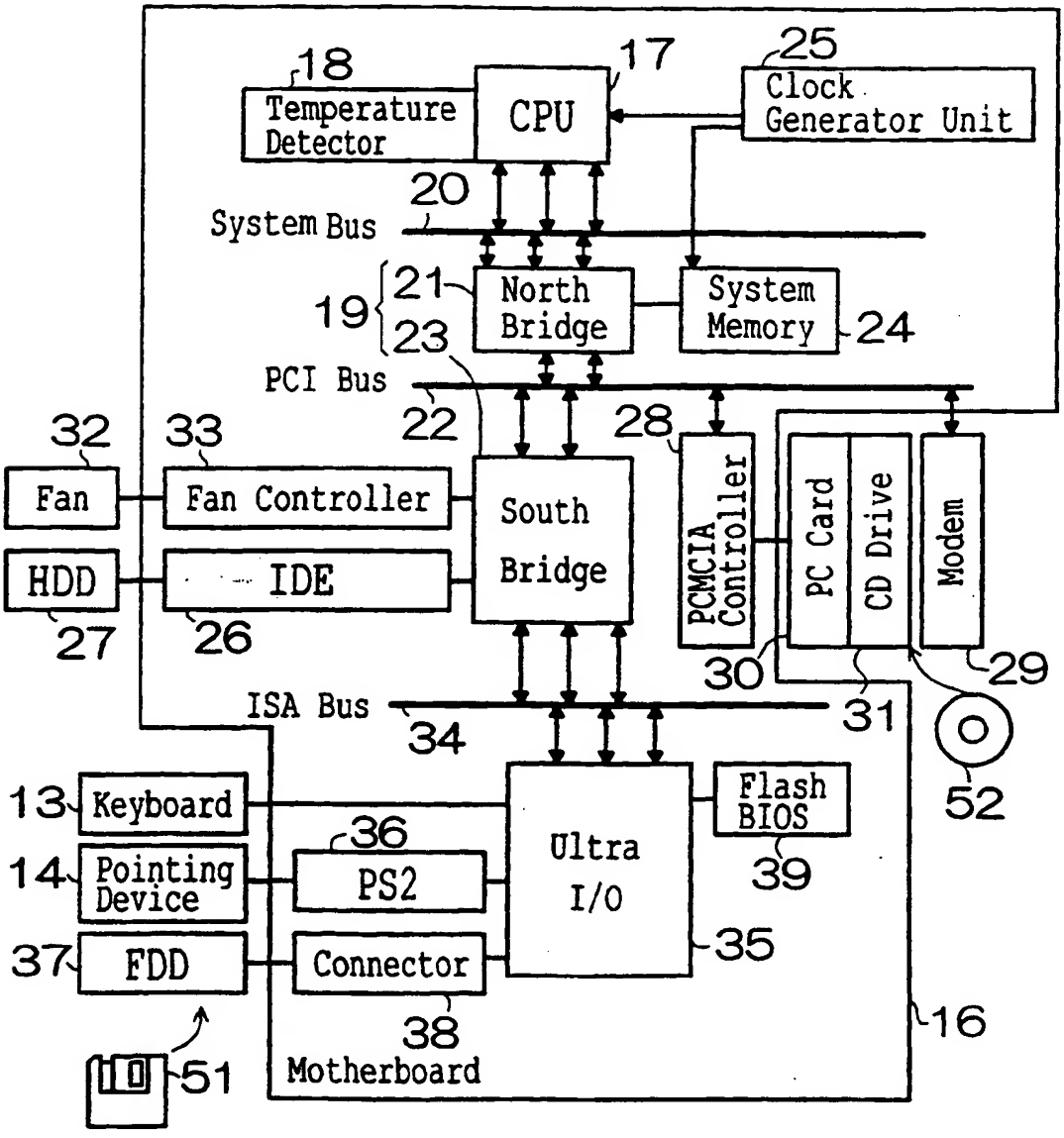

Fig.2

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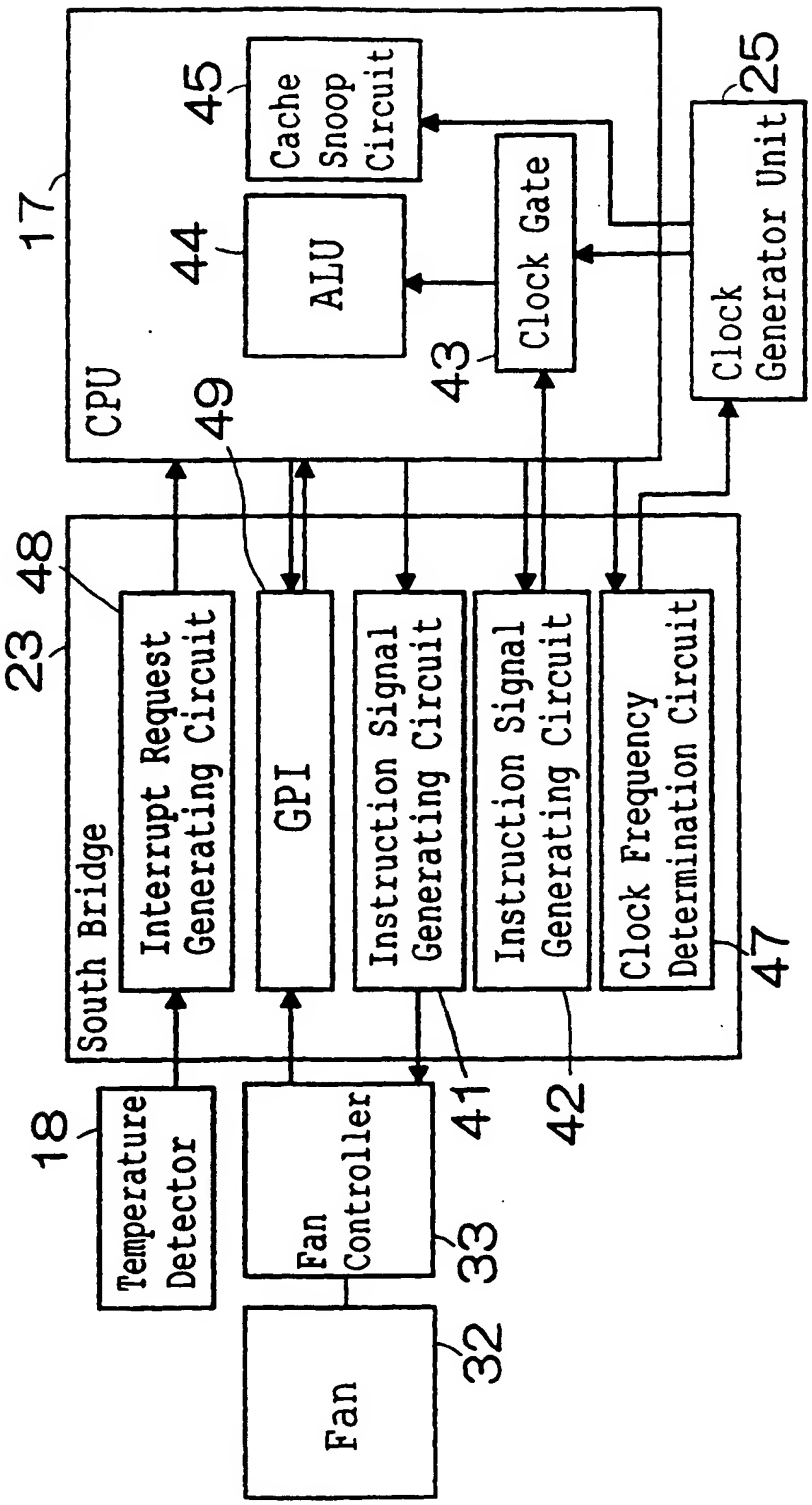

Fig. 3

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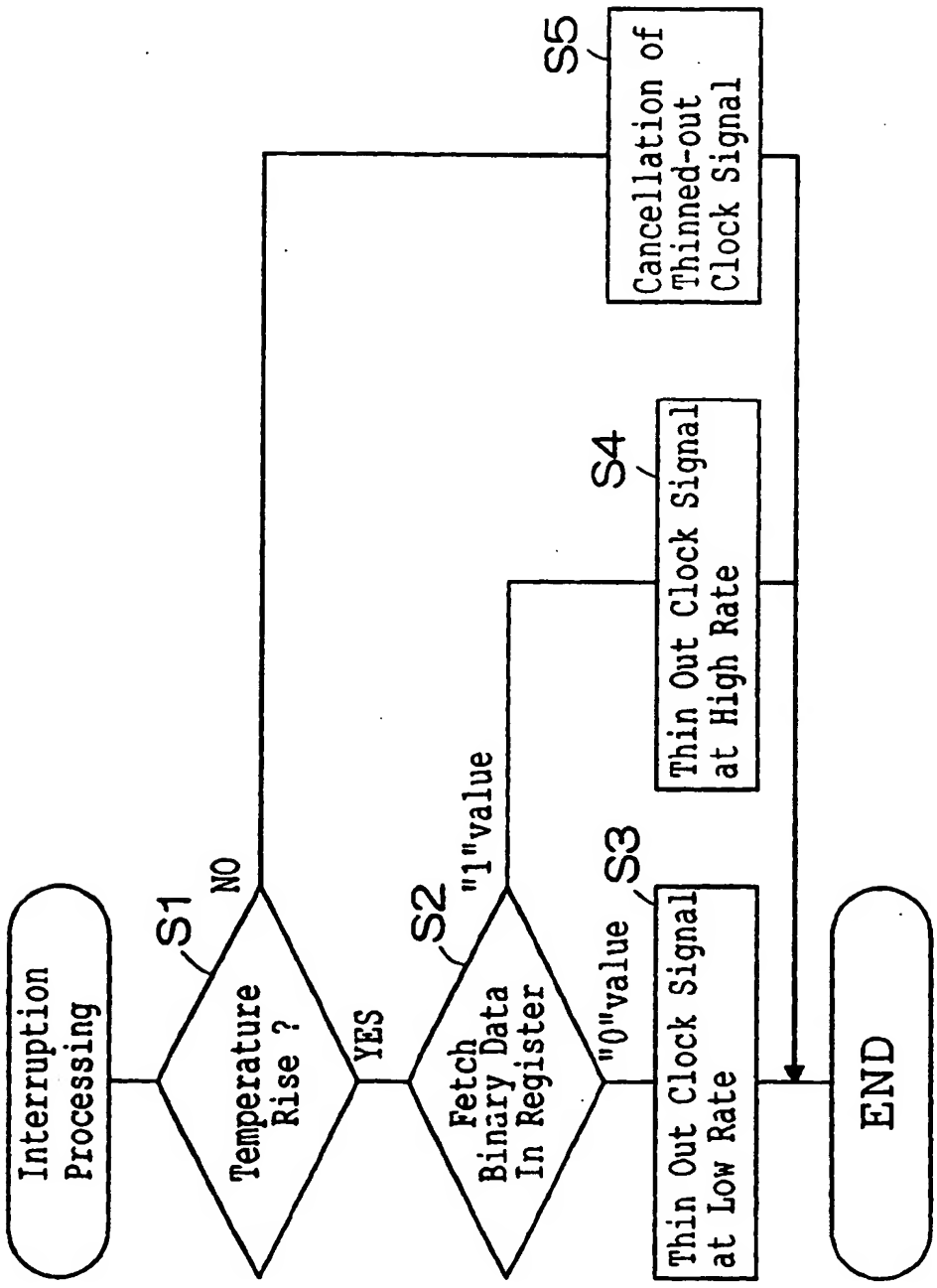

Fig. 4

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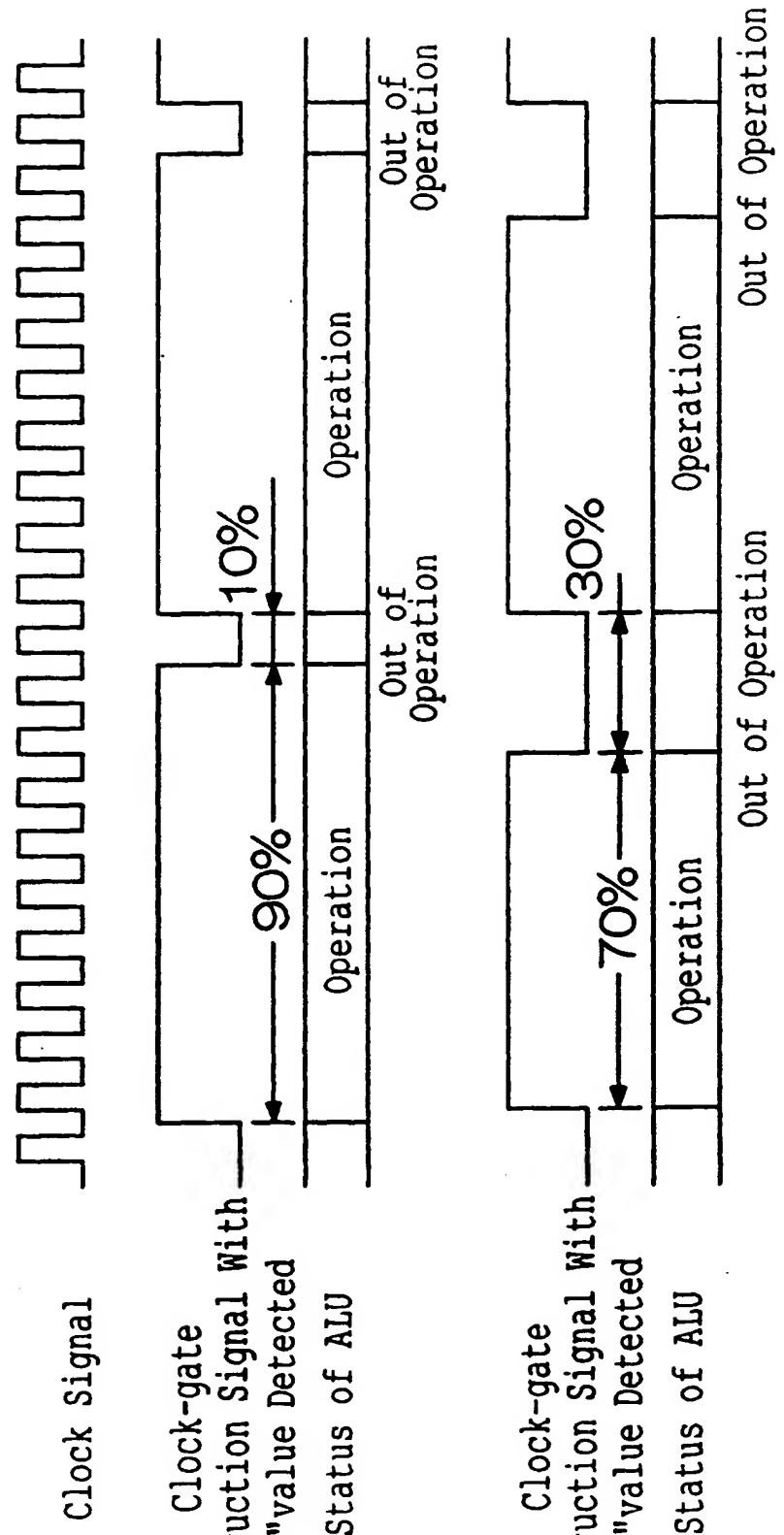

Fig. 5

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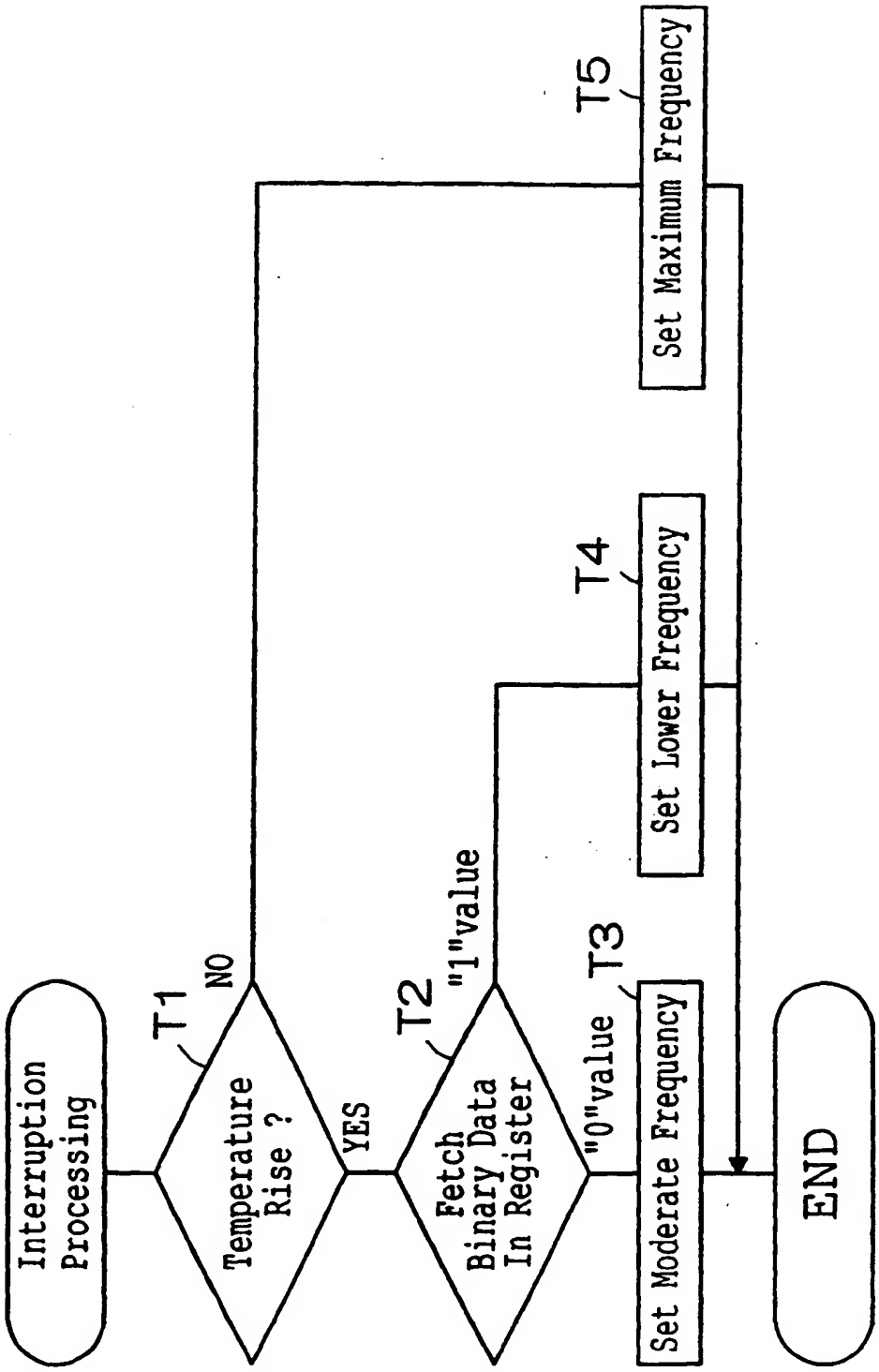

Fig.6

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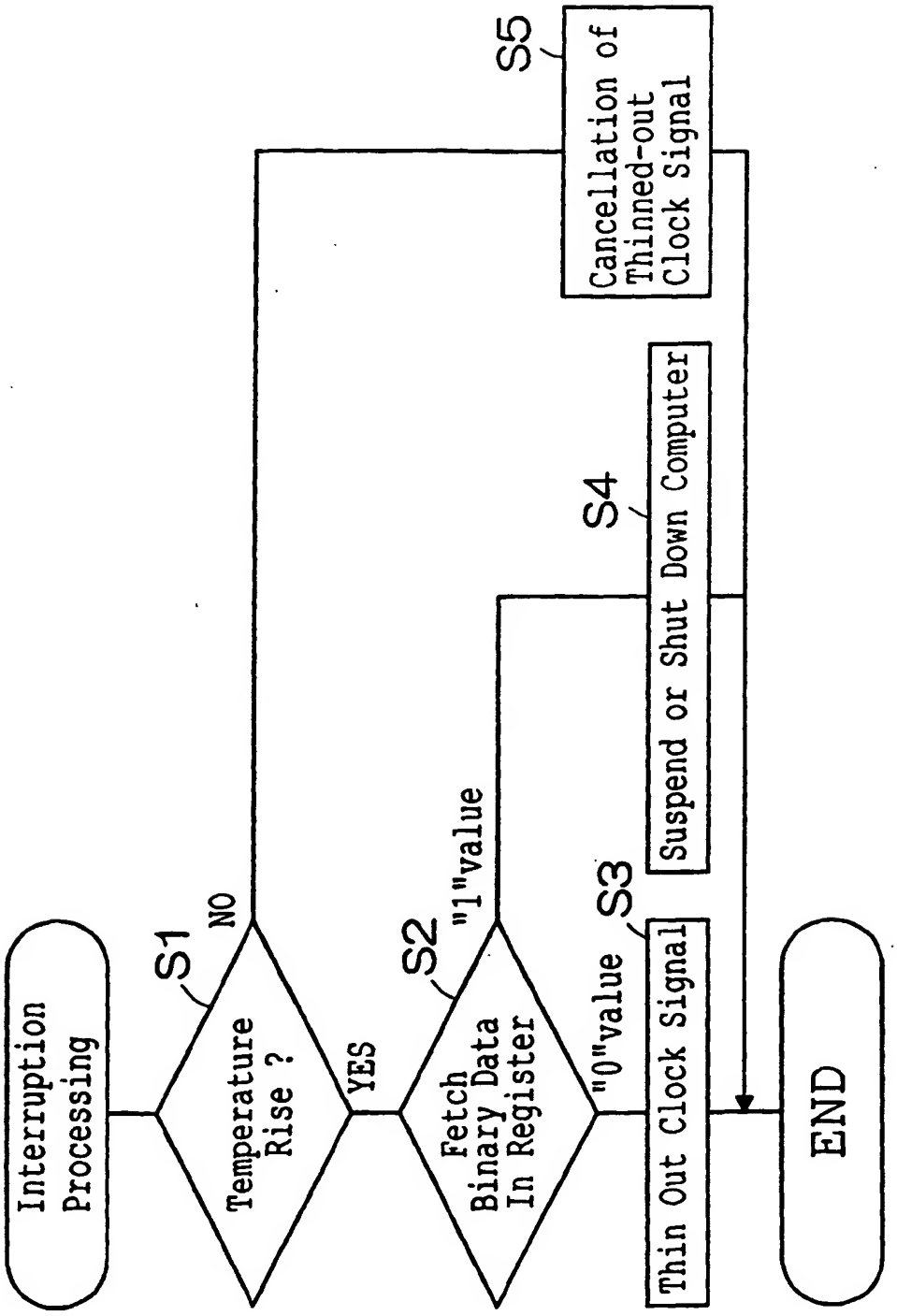

Fig. 7

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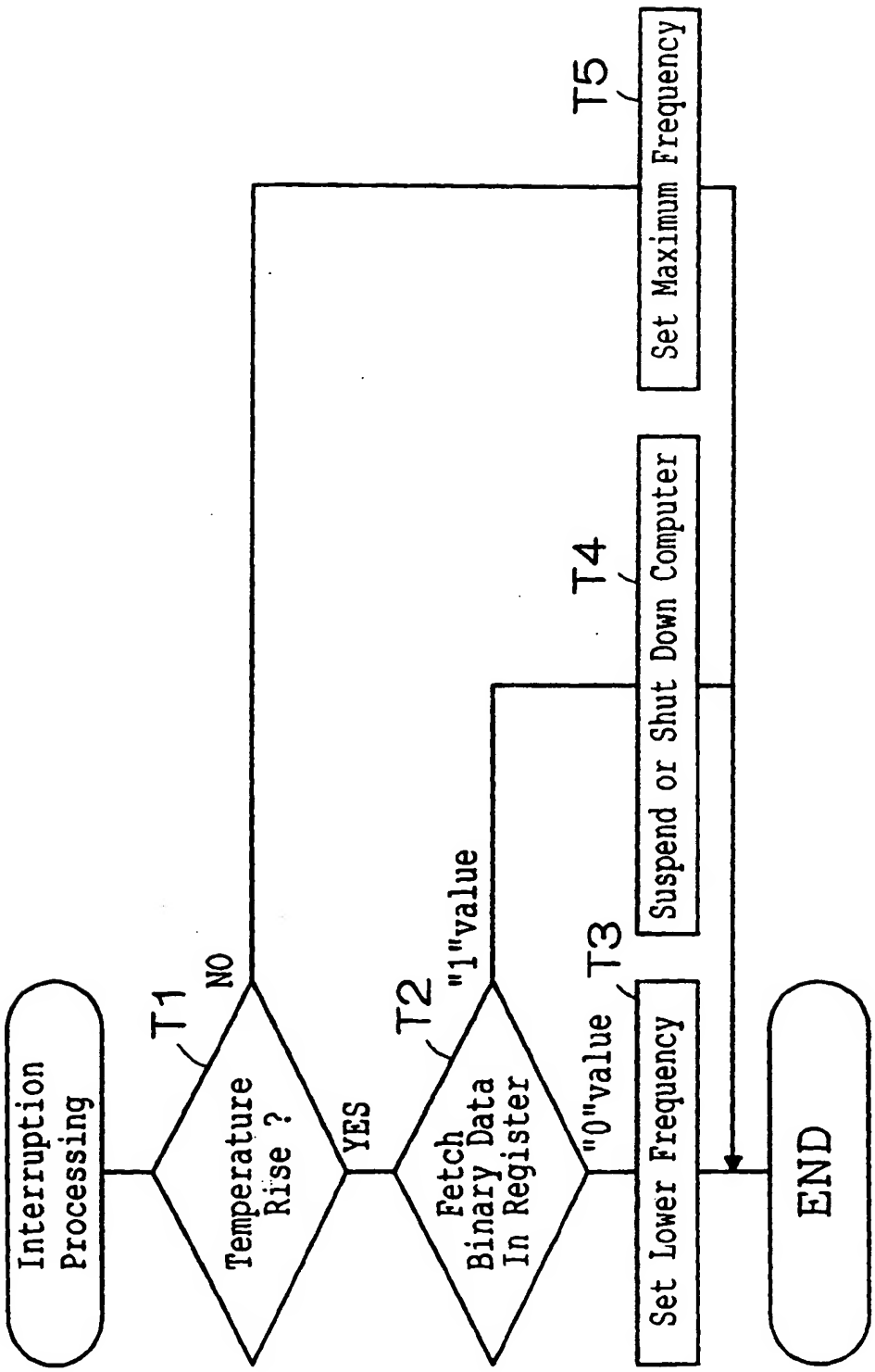

Fig.8

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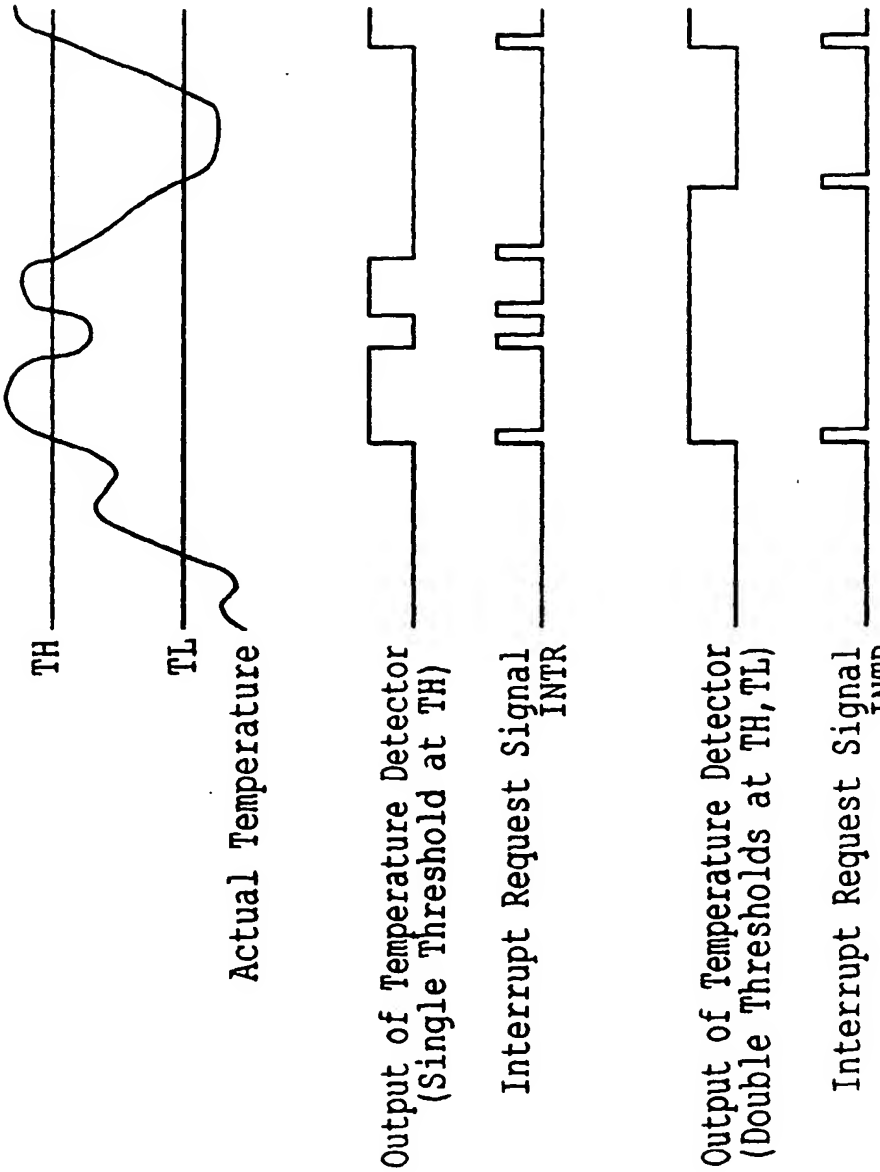

Fig.9

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European Patent Office

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Application Number
EP 00 30 2619

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A	US 5 907 689 A (TAVALLEI ET AL.) 25 May 1999 (1999-05-25) * column 30, line 66 - column 31, line 38; figure 4 *	1,5,9,10	G06F1/20
A	EP 0 840 226 A (COMPAQ COMPUTER CORP.) 6 May 1998 (1998-05-06) * page 3, line 7 - line 40 * * page 4, line 13 - line 52; figures 1,3,20 *	1,5,9,10	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	9 October 2000	Taylor, P

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